

CAD for VLSI 1

Homework #5

1. In this homework, you take the Matrix multiplier designed in Homework #3 and put it through the FPGA tool flow. The specifications for the matrix multiplier are to be taken from Homework #3. Additionally, the following design constraints are to be used:

1. The design must run at 50 MHz (or any appropriate maximum clock frequency available on the board).
2. You must take the size of the matrices to be multiplied from an external input. You may store larger matrices in FPGA internal memory ahead of time. You will use sub-matrices of the size specified in the actual multiplication here.
3. The result of the matrix multiplication must produce the results one after another at 1 Hz. The results must be produced in the row major format.

For acquiring the inputs, you can use a combination of the DIP switches and the pushbuttons on the board. Use the board's manual for figuring out the pin configuration. One way in which you can acquire inputs is to set up the count on the DIP switch first and use a pushbutton switch (let's call it SW1) to take the value. Following this, you give one number at a time using the DIP switch and use the SW1 switch to indicate the availability of a new number. You can use the DIP switch one last time to bootstrap the multiplier into starting the multiplication. The end of multiplication operation can be indicated by a blinking LED after which you can start the display of the matrix entries. It is always a good idea to repeat the outputs forever so that the entries can be noted down slowly.